## REMARKS

Claims 1 through 55 are currently pending in the application.

Claims 6 through 55 are withdrawn from consideration as being directed to a non-elected invention.

Claims 1 through 5 are rejected.

Claims 1 through 3, and 5 have been amended.

This amendment is in response to the Final Rejection in the Office Action of May 13, 2004.

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on D'Souza (U.S. Patent 5,323,107) in view of Bierig (U.S. Patent 4,089,734) and further in view of Rostoker et al. (U.S. Patent 5,838,163), Degani et al. (U.S. Patent 6,370,766) and Piccone et al. (U.S. Patent 3,581,160)

Claims 1 through 3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over D'Souza (U.S. Patent 5,323,107) in view of Bierig (U.S. Patent 4,089,734) and further in view of Rostoker et al. (U.S. Patent 5,838,163) , Degani et al. (U.S. Patent 6,370,766) and Piccone et al. (U.S. Patent 3,581,160). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

The D'Souza reference teaches a probe card having integral test circuitry directly attached to the probe card. A number of registers formed into cells are integrated into an integrated

circuit. To orient the cells, the active probe card is driven with a specific set of high current signals to "burn out" a number of fuses associated with each cell. The pattern of fuses which are retained determines the orientation of the cells. It is not critical that fuses be used to determine the orientation of the cells. A number of shift registers can be incorporated into the adapter circuit as part of the Test Data Register to select the orientation of the cells as instructed by the instruction register.

Turning to the Bierig reference, a fusing technique is described where a fuse is fabricated upon a substrate by integrated circuit techniques. The fuses are useful in applications such as microwave diode power amplifiers used in phased array radar systems and in read only memories and memory reconfiguration applications wherein a plurality of diodes is connected in parallel in each amplifier. In such a connection, if one of the diodes fails by short-circuiting and there is no protection, the entire amplifier also fails and becomes inoperative. By inserting a fuse in series with the DC bias connection to each of these diodes, a single diode failure will not result in catastrophic failure of the entire amplifier. In the fusing technique, three or more layers of chemically dissimilar metals are deposited upon the region where the fuse is to be formed. The top layers are then etched away from the region where the fusible link is to be formed leaving the lower tow layers, the top one of which forms the actual fusible link. The lower layer is then etched away leaving the fusible link suspended from the underlying substrate.

The Piccone reference teaches a high-current semiconductor rectifier device including a disc like body 12 made of semiconductor material sandwiched under pressure between opposing electrodes of a sealed housing. A rectifier is used to convert alternating current into direct current. A high current semiconductor device may sometimes fail, one cause being excessive surge currents. The failure mechanism typically includes overheating localized areas of the silicon wafer which then lose blocking ability and permit the unimpeded flow of reverse current. This will usually occur near the center of the wafer where short circuit current is well contained and will not cause permanent damage outside the afflicted device itself. (Col. 1 lines 26-35) The *external* electric circuit will ordinarily include suitable protective means such as an electric fuse to *isolate the failed device which can then be replaced* by a new one. (Col. 5 lines 14-18)

The Degani reference teaches a batch testing technique for PC cards. Final testing, including burn-in if required, is completed prior to applying the epoxy underfill because after the epoxy underfill is applied it becomes difficult and impractical to replace defective component packages during final assembly. Burn-in testing means applying an electrical bias or signal to the components with the components subjected to elevated temperatures combined with elevated humidity.

Applicant asserts that any combination of the combination of the D'Souza, Bierig, Rostoker, Piccone, and Degani references do not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of independent claim 1, as proposed to be amended herein, because, at the very least, the cited references do not teach or suggest all of the claim limitations of the presently claimed invention and the references do not suggest the presently claimed invention or set forth any reasonable expectation of success based upon any disclosure set forth therein.

Applicant asserts that the cited references do not teach or suggest the claim limitations of the presently claimed inventions of independent claim 1, as amended herein, calling for a method of forming a probe card for use in the testing of a semiconductor device comprising . . . "providing a substrate having a first surface, a second surface, and an aperture therethrough", "disposing a plurality of conductive traces adjacent at least one of the first surface and the second surface", "providing a plurality of probe elements in electrical communication with the plurality of conductive traces, at least a first one of the probe elements configured for supplying a test signal, and at least a second one of the probe elements configured for receiving a test signal, the plurality of probe elements having a portion thereof located on the first surface of the substrate, having a portion thereof extending through an aperture in the substrate, and having a portion thereof located on the second surface of the substrate", "providing a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent the at least one of the first surface and the second surface, at least some of the plurality of *fuse elements comprising at least two types of fuses* of an active fuse element, a passive fuse element, a self-resetting fuse element, a repairable fuse element, and a replaceable fuse element, each fuse element of the

plurality of fuse elements for *limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute current level for use in the testing of a semiconductor device without substantial damage thereto.*" (emphasis added) The D'Souza reference teaches probe elements located on only one side of the substrate. Additionally, Degani teaches fuse elements patterned to determine the orientation of the cells in an integrated circuit. Bierig teaches fuse elements in applications such as microwave diode power amplifiers used in phased array radar systems and in read only memories and memory reconfiguration applications. The Piccone reference teaches an electric fuse used in an *external* electric circuit to *isolate a failed device which can be replaced* by a new one. The Degani reference teaches a batch testing technique including burn-in testing to *identify defective component packages*.

Applicant asserts that nowhere in the cited reference is there any description whatsoever to the elements of the invention of independent claim 1, as amended herein. Accordingly, the D'Souza, Bierig, Rostoker, Piccone, and Degani references cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the invention of independent claim 1, as proposed to be amended herein.

Claims 2 through 3 and 5 are each allowable, among other reasons, as depending from claim 1 which should be allowed.

Additionally, Applicant asserts that there is no suggestion whatsoever in the cited references for any combination or modification thereto for any of the claim limitations set forth in claims 1 through 3 and 5 or for any success in the combination or modification of the references. Any such suggestions come solely from the Applicant's disclosure not the cited prior art references. The fuses of the D'Souza reference are used to orient the cells by "burning out" a number of fuses associated with each cell while the probe elements only extend from one side of the substrate. One of ordinary skill in the art would have no reasonable expectation of success for the modification of the fuses of the D'Souza reference with an active fuse element, a self-resetting fuse element, or a repairable fuse element. Further, there is no motivation to modify the fuses of the D'Souza reference for limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute

current level for use in the testing of a semiconductor device without substantial damage thereto. Accordingly, the references cannot and do not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of claims 1 through 3 and 5.

Obviousness Rejection Based on D'Souza (U.S. Patent 5,323,107)/Bierig (U.S. Patent 4,089,734)/Rostoker et al. (U.S. Patent 5,838,163)/Degani et al. (U.S. Patent 6,370,766)/Piccone et al. (U.S. Patent 3,581,160) as applied to claims 1 and 3 above, and further in view of Maruyama et al. (U.S. Patent 5,832,595)

Claims 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over D'Souza (U.S. Patent 5,323,107)/Bierig (U.S. Patent 4,089,734)/Rostoker et al. (U.S. Patent 5,838,163)/Degani et al. (U.S. Patent 6,370,766) and Piccone et al. (U.S. Patent 3,581,160) as applied to claims 1 and 3 above, and further in view of Maruyama et al. (U.S. Patent 5,832,595). Applicant respectfully traverses this rejection, as hereinafter set forth.

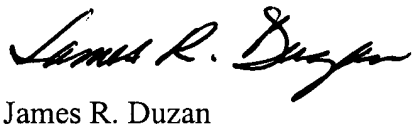
Applicant again asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Claim 4 is allowable, among other reasons, as depending from claim 1 which should be allowed, as set forth hereinabove.

## ENTRY OF AMENDMENTS

The amendments to claims 1 through 3 and 5 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

Respectfully submitted,



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